NEX83288

Transition mode boost Power Factor Correction controller

Rev. 1.1 — 16 September 2025 Product data sheet

1. General description

NEX83288 is a Power Factor Correction (PFC) controller. It supports transition mode (CrM/DCM) operations.

The device uses average current mode based VOT-control to achieve high power factor and low-current total harmonic distortion (THD) over a wide line voltage. The device features a very low supply current in burst mode. This allows the device to achieve low standby power loss.

The switching frequency near the line voltage zero cross region is reduced by the control method. It improves efficiency.

NEX83288 features overvoltage protection (OVP), cycle-by-cycle (CBC) current limit, open-loop protection (OLP), overtemperature protection (OTP), brown-in and brown-out.

NEX83288 is available in SO8 package.

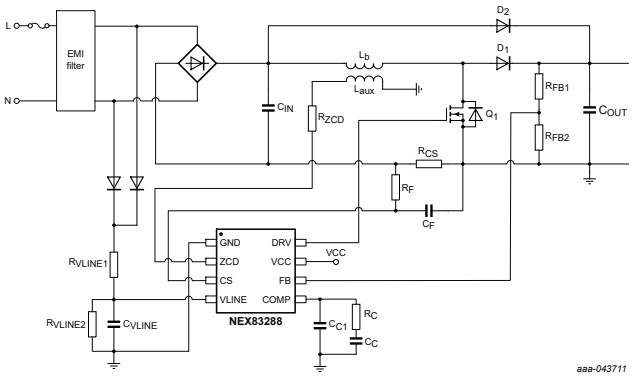


Fig. 1. Typical application

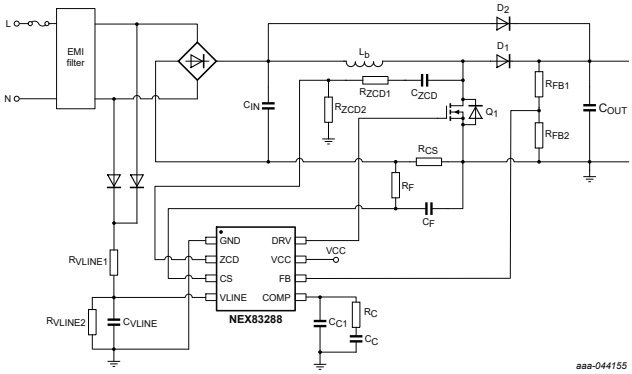


Fig. 2. Typical application without auxiliary winding

2. Features and benefits

- Adaptive variable on time control
- Transition mode (CrM/DCM) operations
- Supports E-mode GaN HEMT direct drive
- Line voltage feed forward
- Integrated THD enhancement circuit
- Integrated dynamic enhancement circuit
- Maximum switching frequency clamp to reduce the losses
- Valley/zero-voltage switching for minimum switching losses
- Rich protections:
  - VCC UVLO/OVP
  - Output OVP
  - Cycle-by-cycle (CBC) current limit
  - Open-loop protection (OLP)
  - Overtemperature protection (OTP)
  - Brown-in/brown-out
- Available in SO8 package

3. Applications

- Monitors or LCD televisions
- Personal computer power adapters
- USB Power Delivery quick chargers
- All off-line appliances requiring power factor correction

Table 1. Device information

Part number	Package	Body size
NEX83288	SO8	4.9 mm x 3.9 mm x 1.75 mm

nexperia

4. Ordering information

Table 2. Ordering information

Type number	Temperature range (T_j)	Name	Description	Version
NEX83288D	-40 °C to 150 °C	SO8	plastic, small outline package; 8 leads; 1.27 mm pitch; 4.9 mm x 3.9 mm x 1.75 mm body	SOT96-2

5. Marking

Table 3. Marking code

Type number	Marking code
NEX83288D	N83288

6. Pin configuration and description

6.1. Pin configuration

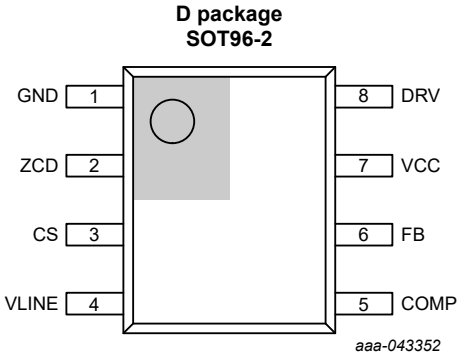


Fig. 3. NEX83288 pin diagram

6.2. Pin description

Symbol	Pin	I/O	Description
GND	1	PWR	GND supply pin
ZCD	2	IN	input from auxiliary winding for demagnetization timing and valley detection for PFC
CS	3	IN	current sense input for PFC
VLINE	4	IN	sense input for line voltage
COMP	5	OUT	loop compensation pin; the compensation network is connected between this pin and GND
FB	6	IN	output voltage sense pin
VCC	7	PWR	supply voltage
DRV	8	OUT	gate driver output pin

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
VCC	supply voltage		-0.3	40	V
V_{ZCD}	pin voltage	current limited	-0.3	6.5	V
V_{CS}		current limited	-1	5.5	V
V_{VLINE}		current limited	-0.3	5.5	V
V_{COMP}		current limited	-0.3	5.5	V
V_{FB}		current limited	-0.3	5.5	V
V_{DRV}		current limited	-0.3	13	V
T_j	junction temperature		-40	150	°C
T_{stg}	storage temperature		-65	150	°C

[1] Stresses beyond those conditions under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	-	2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	-500	-	500	V

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
VCC	supply voltage		14	33	V
V_{VLINE}	sensed line voltage		0	5	V
T_j	junction temperature		-40	125	°C

10. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	SOT96-2 (SO8)	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	160	°C/W
$R_{\Theta JC(top)}$	junction-to-case (top) thermal resistance	85	°C/W
$R_{\Theta Jb}$	junction-to-board thermal resistance	125	°C/W
Φ_{JT}	junction to top char parameter	39	°C/W

11. Electrical characteristics

Table 8. Electrical characteristics

Where VCC = 18 V; typical values are measured T_j = 25 °C (unless otherwise noted).

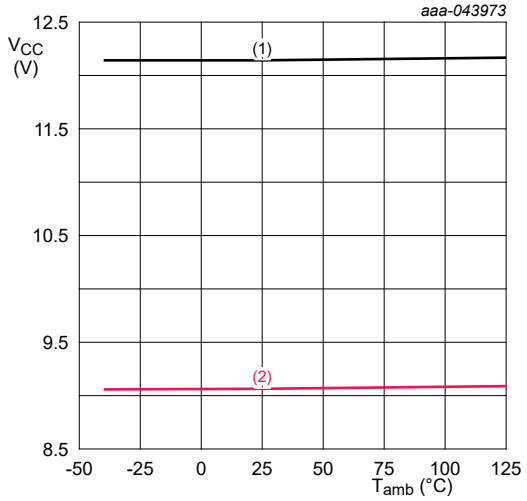
Symbol	Parameter	Conditions	T_j = -40 °C to 125 °C			Unit
			Min	Typ	Max	
Supply (VCC pin)						
V_{VCC_ON}	VCC on threshold voltage	VCC rising	11.4	12	12.8	V
V_{VCC_OFF}	VCC off threshold voltage	VCC falling	8.5	9	9.5	V
$V_{VCC\_OVP\_H}$	over voltage protection voltage high threshold	VCC rising	33.5	36	39.3	V
$V_{VCC\_OVP\_L}$	over voltage protection voltage low threshold	VCC falling	31	34	37.5	V
$I_{VCC\_STARTUP}$	operating current during normal operation	VCC = 9.5 V during start-up	-	-	120	µA
I_{VCC_Q}	operating quiescent current	DRV pin is floating, or device is non-switching	-	0.45	0.63	mA
I_{VCC_NOM}	VCC normal operating current	f_{SW} = 89 kHz; C_{Load} = 1 nF on DRV pin	-	1.5	3.8	mA
		f_{SW} = 135 kHz; C_{Load} = 1 nF on DRV pin	-	4.6	6.2	mA
		f_{SW} = 260 kHz; C_{Load} = 1 nF on DRV pin	-	5	7.5	mA
Gate driver output (DRV pin)						
I_{DRV_SOURCE}	DRV source current capability	V_{DRV} = 2 V; V_{VCC} ≥ 12 V	-	-0.6	-	A
I_{DRV_SINK}	DRV sink current capability	V_{DRV} = 10 V; V_{VCC} ≥ 12 V	-	1.4	-	A
V_{DRV_MAX}	maximum DRV voltage for MOSFET and D-mode GaN FET		11.1	12	13	V
	maximum DRV voltage for E-mode GaN FET		5.56	6.08	6.78	V
t_R	voltage rising time for MOSFET	C_{Load} = 1 nF; 10% to 90% of output signal	-	63	-	ns
	voltage rising time for GaN FET	C_{Load} = 150 pF; 10% to 90% of output signal	-	56	-	ns
t_F	voltage falling time for MOSFET	C_{Load} = 1 nF; 10% to 90% of output signal	-	16.5	-	ns
	voltage falling time for GaN FET	C_{Load} = 150 pF; 10% to 90% of output signal	-	2.3	-	ns
f_{sw_max}	maximum switching frequency	middle frequency version	115	135	155	kHz
Zero-current detection (ZCD pin)						
V_{ZCD_DETA}	zero-current detection arming threshold voltage on ZCD pin	MOSFET	1.9	2.1	2.3	V
		GaNFET	1.34	1.4	1.43	V
V_{ZCD_DETT}	zero-current detection trigger threshold voltage on ZCD pin	MOSFET	1.44	1.4	1.76	V
		GaNFET	0.64	0.7	0.755	V

Symbol	Parameter	Conditions	T_j = -40 °C to 125 °C			Unit
			Min	Typ	Max	
I_{ZCD_DET}	protection current for ZCD		5	-	-	mA
t_{TIME_OUT}	zero-current detection arming time-out time		-	30	-	µs
$V_{ZCD\_CLAMP\_H}$	upper voltage clamp on ZCD pin		5.13	5.70	6.27	V
$V_{ZCD\_CLAMP\_L}$	lower voltage clamp on ZCD pin	MOSFET	5.35	5.8	6.55	V
		GaNFET	0	0.32	0.55	V
t_{ZCD_DELAY}	turn-on delay after ZCD detected	MOSFET	-	100	-	ns
		GaNFET	-	50	-	ns
Current sensing (CS pin)						
V_{CBC_OCP}	inductor saturation protection threshold	enable CBC function	-0.55	-0.49	-0.44	V
Line voltage detection (VLINE pin)						
V_{LINE_BI}	brown-in voltage threshold		0.698	0.750	0.802	V
V_{LINE_BO}	brown-out voltage threshold		0.500	0.550	0.600	V
$V_{BO(HYS)}$	brown-out comparator hysteresis		-	0.2	-	V
$V_{LINE\_TH\_HL}$	high line detection threshold		1.57	1.65	1.73	V
$V_{LINE\_TH\_LL}$	low line detection threshold		1.38	1.45	1.52	V
$t_{LINE\_DET\_DB}$	the debounce time from high line to low line detection		-	50	-	ms
$V_{LINE\_AC\_DROP}$	AC drop start detection threshold		0.20	0.25	0.30	V
	AC drop stop detection threshold		0.34	0.4	0.45	V
t_{AC_DROP}	AC drop detection time		-	5	-	ms
t_{BO_DB}	brown-out detection debounce time		-	50	-	ms
Regulation and compensation (COMP pin)						
V_{REF}	output reference voltage		2.463	2.500	2.550	V
$G_{m(low)}$	transconductance	V_{FB} = 2.25 V to 2.35 V	100	400	750	µA/V
$G_{m(normal)}$		V_{FB} = 2.45 V to 2.55 V	132	160	185	µA/V
$G_{m(high)}$		V_{FB} = 2.6 V to 2.7 V	1050	1500	1870	µA/V
I_{COMP_source}	source current on COMP pin	V_{FB} < 2.1 V at normal operation	70	125	180	µA
		V_{FB} = 2.45 V at normal operation	1	8	16	µA
		TM version during startup	18	30	42	µA
		MM version at high line during startup	36	57	78	µA
		MM version at low line during startup	12	24	42	µA
I_{COMP_sink}	sink current on COMP pin	V_{FB} = 2.55 V	-12.5	-8.6	-4.75	µA
		V_{FB} = 2.65 V	-143	-98	-55	µA

Symbol	Parameter	Conditions	T_j = -40 °C to 125 °C			Unit
			Min	Typ	Max	
V_{COMP_clamp}	clamp voltage on COMP pin	upper clamp voltage; unidirectional clamp; operating mode; PFC on;	3.1	3.5	3.9	V
		lower clamp voltage; unidirectional clamp; operating mode; PFC on;	0.29	0.35	0.41	V
V_{BURST_TH}	burst mode voltage threshold		0.470	0.500	0.535	V
Output voltage sensing (FB pin)						
$V_{FB\_OLP\_H}$	open-loop protection threshold		0.42	0.50	0.58	V
$V_{FB\_OLP\_L}$			0.34	0.40	0.47	V
t_{OLP_R}	OLP recovery time		-	219	-	ms
t_{OLP_DB}	open-loop protection debounce time		-	50	-	µs
t_{DELAY_START}	start-up delay time	after open-loop protection removed	-	5	-	ms
$V_{FB\_OVP\_H}$	overvoltage protection threshold		2.64	2.70	2.77	V
$V_{FB\_OVP\_L}$			2.5	2.6	2.7	V
t_{OVP_DB}	overvoltage protection debounce time		-	20	-	µs
I_{FB_FOLLOW}	FB source current for following boost		18	20	22	µA
$t_{transition}$	following boost transition time		-	30	-	ms
Overtemperature protection (internal OTP)						
T_{OTP}	OTP trigger level		-	150	-	°C
T_{OTP_HYS}	OTP hysteresis		-	50	-	°C

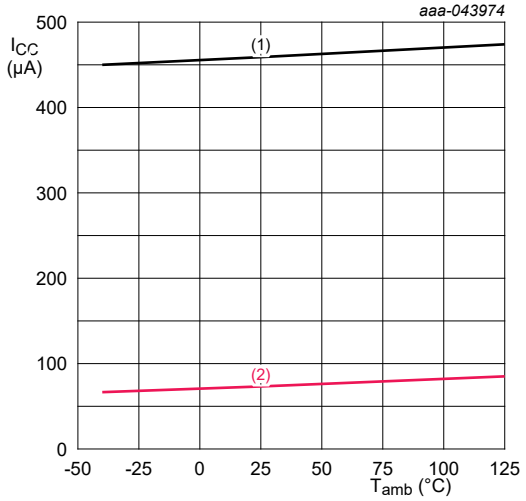
12. Typical characteristics

Table 9. Typical characteristics



(1) VCC_ON
(2) VCC_OFF

Fig. 4. VCC_ON and VCC_OFF vs ambient temperature



(1) ICC_START
(2) ICC_Q

Fig. 5. I_{CC} vs ambient temperature

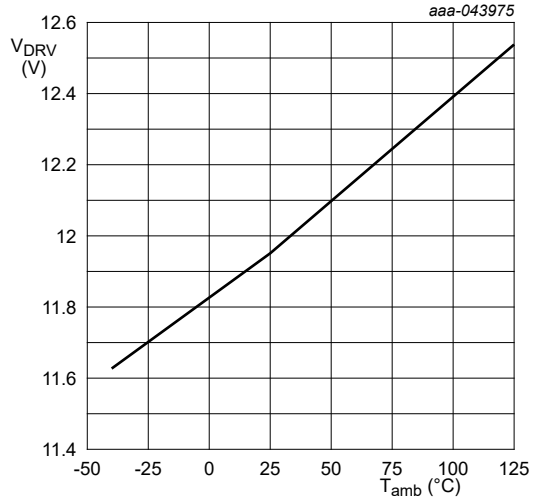


Fig. 6. V_{DRV} vs ambient temperature

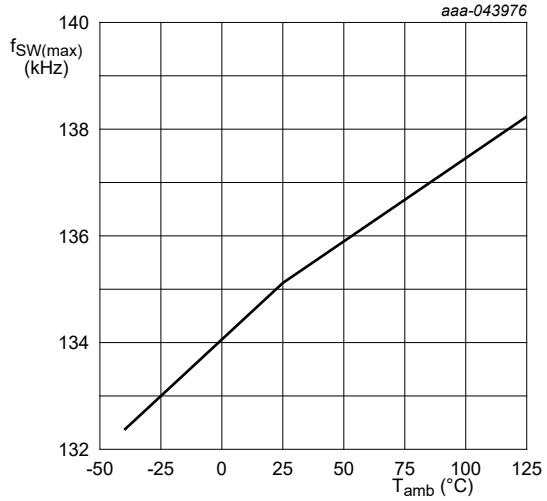
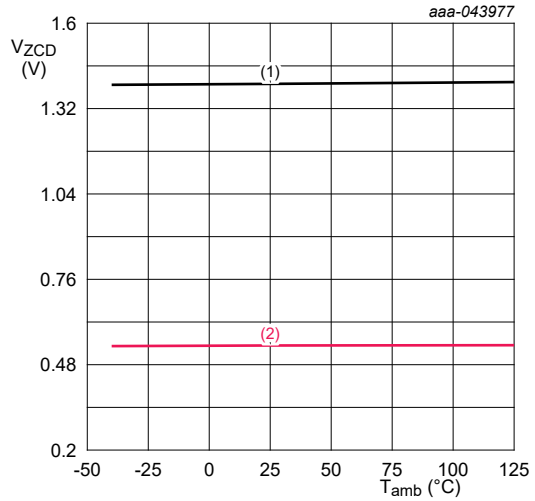


Fig. 7. f_{SW_max} vs ambient temperature



(1) V_{ZCD_DETA}
(2) V_{ZCD_DETT}

Fig. 8. V_{ZCD_DETA} and V_{ZCD_DETT} vs ambient temperature

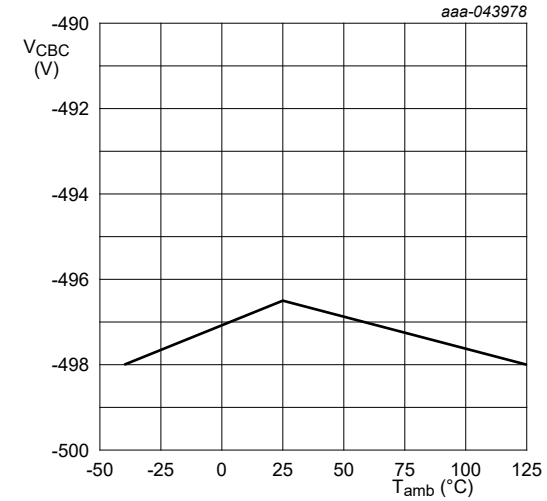
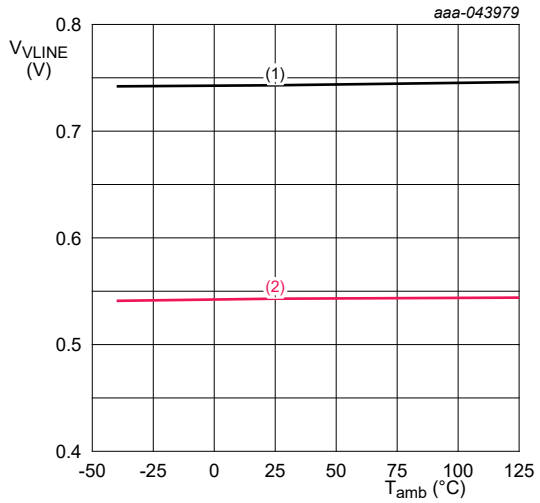
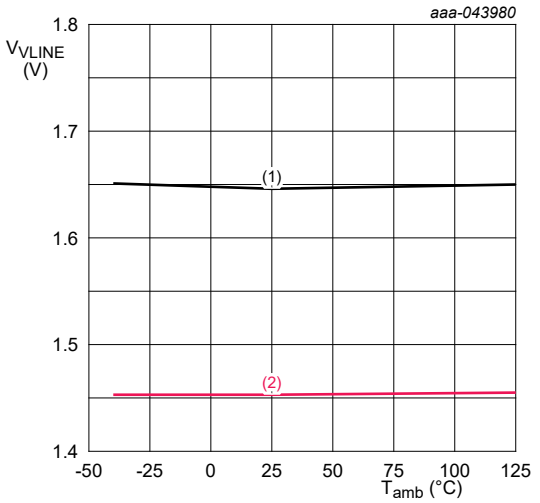


Fig. 9. V_{CBC_OCP} vs ambient temperature



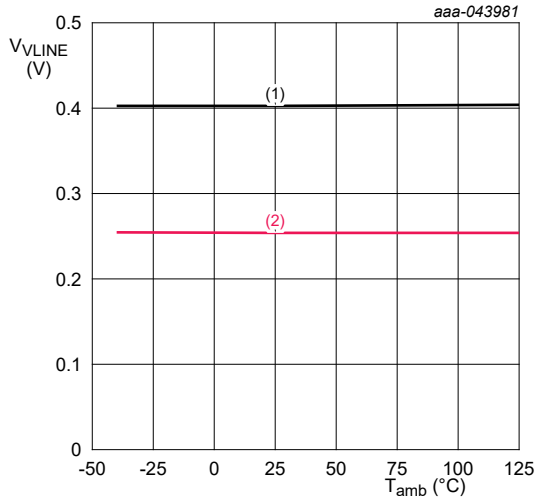
(1) V_{VLINE_BI}
(2) V_{VLINE_BO}

Fig. 10. V_{VLINE_BI} and V_{VLINE_BO} vs ambient temperature



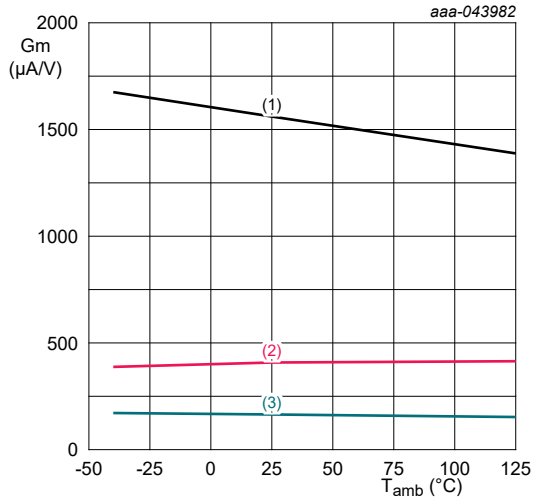
(1) $V_{VLINE\_TH\_HL}$
(2) $V_{LINE\_TH\_LL}$

Fig. 11. $V_{VLINE\_TH\_HL}$ and $V_{LINE\_TH\_LL}$ vs ambient temperature



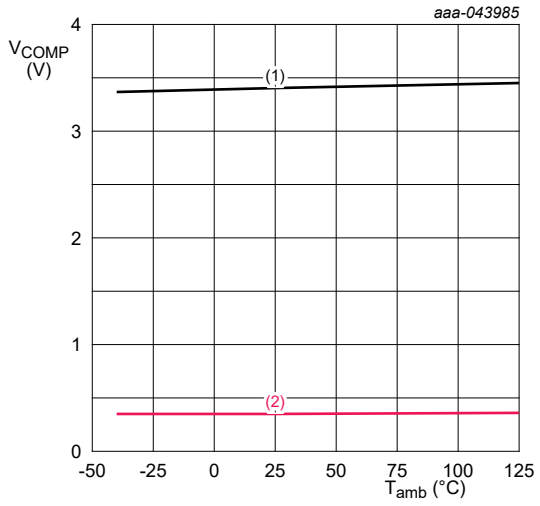
(1) $V_{AC\_DROP\_DET}$
(2) $V_{AC\_DROP\_CLR}$

Fig. 12. $V_{AC\_DROP\_DET}$ and $V_{AC\_DROP\_CLR}$ vs ambient temperature



(1) $G_{m(high)}$
(2) $G_{m(low)}$
(3) $G_{m(normal)}$

Fig. 13. $G_{m(low)}$, $G_{m(normal)}$, $G_{m(high)}$ vs ambient temperature



(1) $V_{COMP\_clamp\_high}$
(2) $V_{COMP\_clamp\_low}$

Fig. 14. V_{COMP_clamp} vs ambient temperature

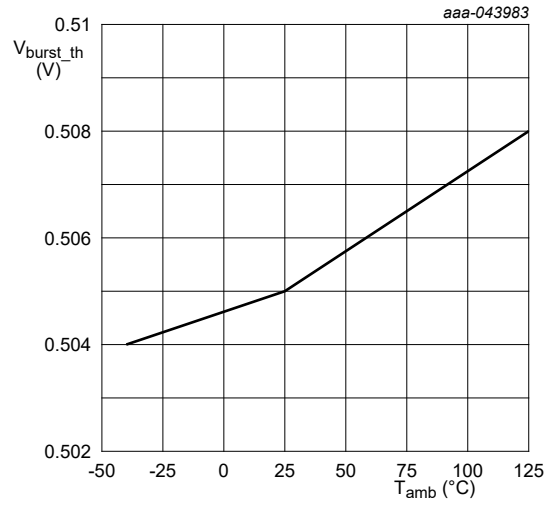
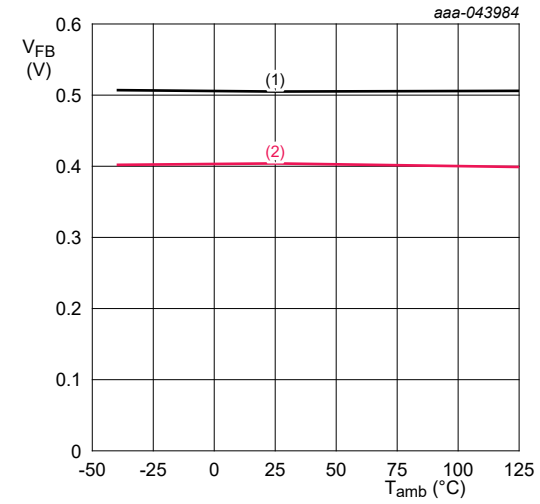
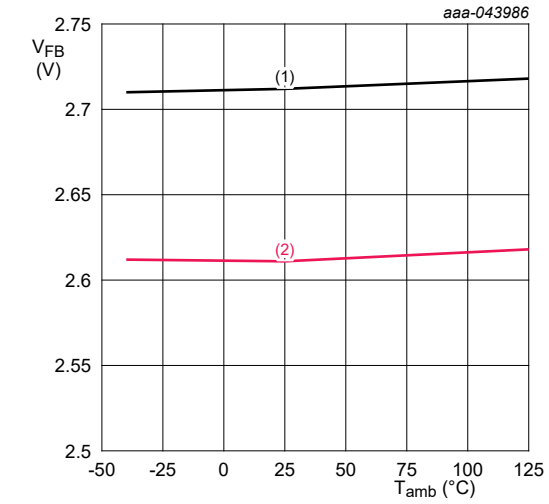


Fig. 15. V_{BURST_TH} vs ambient temperature



(1) $V_{FB\_OLP\_H}$
(2) $V_{FB\_OLP\_L}$

Fig. 16. $V_{FB\_OLP\_H}$ and $V_{FB\_OLP\_L}$ vs ambient temperature



(1) $V_{FB\_OVP\_H}$
(2) $V_{FB\_OVP\_L}$

Fig. 17. $V_{FB\_OVP\_H}$ and $V_{FB\_OVP\_L}$ vs ambient temperature

13. Detailed Description

13.1. Overview

NEX83288 is a boost power factor correction (PFC) controller, which supports transition mode (TM) operation. Using the average current mode (ACM) based on time control technology, the device implements adaptive variable on time (VOT) control to achieve a high PF.

The device supports both MOSFET/D-mode GaN FET and E-mode GaN FET direct drive option. The maximum frequency can reach 135 kHz and 260 kHz respectively for MOSFET and E-mode GaN FET. In addition, it supports 2-level following boost function option.

The device supports line voltage feed forward and integrates a nonlinear transconductance error amplifier circuit to improve the large-scale dynamic response. It also integrates THD enhancement circuit to improve the current distortion.

13.2. Functional block diagram

Fig. 18 shows the functional block diagram of NEX83288:

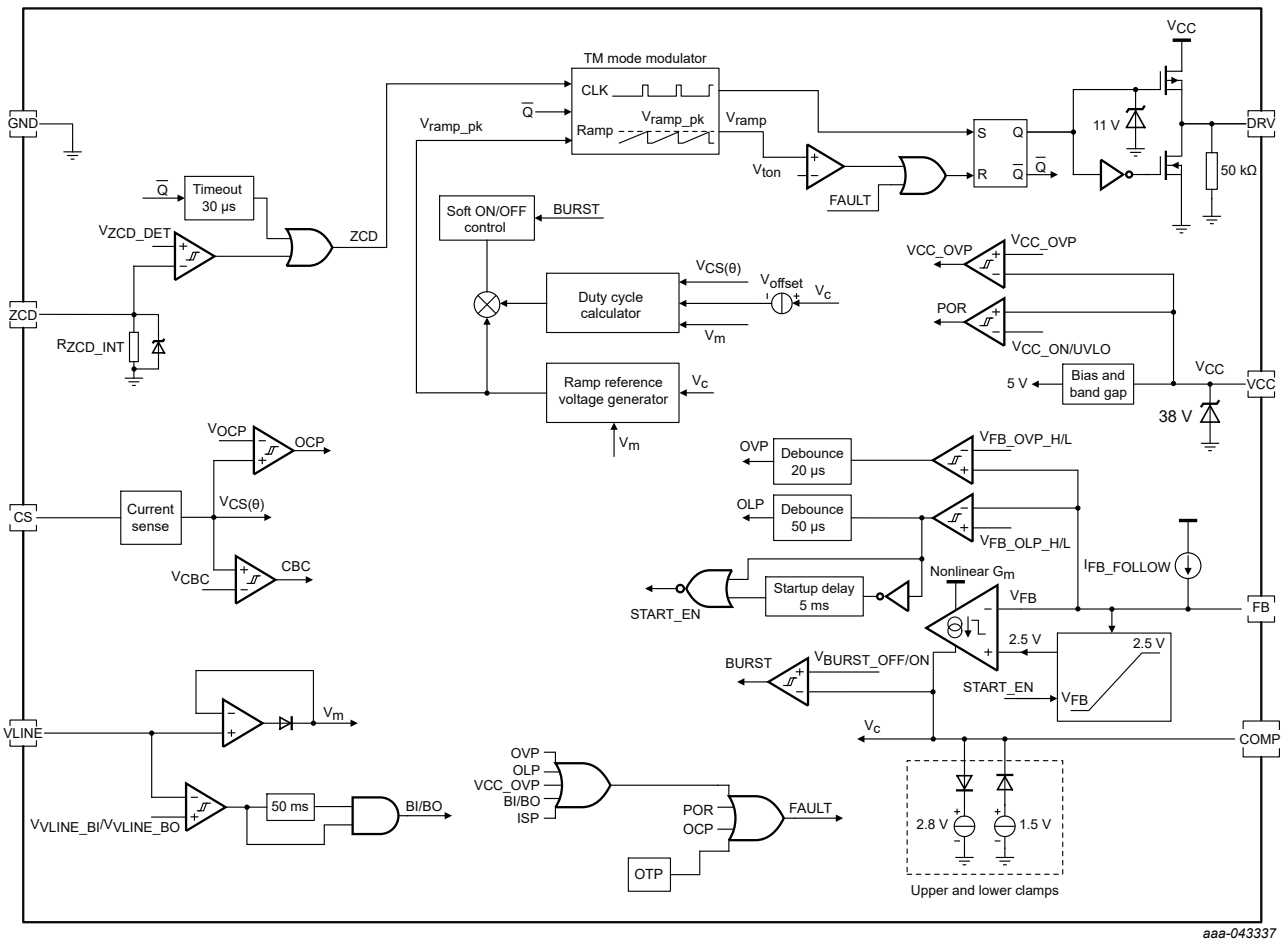


Fig. 18. Functional block diagram

13.3. Feature description

13.3.1. ACM-based On time control

NEX83288 adopts a unified average current mode based on time control technology. Based on Volt-Second balance, the On time is given by equation (1).

$$t_{on}(\theta) = \left[1 - \frac{v_{in}(\theta)}{v_o}\right] T_s \quad (1)$$

Since the PFC converter can adjust the power factor to 1, the input impedance for PFC converter is

$$R_{in\_eq} = \frac{v_{in}(\theta)}{i_{in}(\theta)} \quad (2)$$

According to equation (2), the input current is always tracking the input voltage as long as R_{in_eq} is constant. Combine equation (1) and (2), and the On time is given by

$$t_{on}(\theta) = \left[1 - \frac{R_{in\_eq} i_{in}(\theta)}{v_o}\right] T_s \quad (3)$$

According to equation (3), the On time is related to the input current (inductor current average value). When R_{in_eq} is constant, the input current is always tracking the input voltage. If $\frac{R_{in\_eq}}{v_o}$ is generated by the control loop and $i_{in}(\Theta)$ is the actual input current, the input current will automatically track the input voltage. According to the above analysis, the input current will auto-track the line voltage and achieve a high power factor. For CrM/DCM mode, the actual switching frequency f_{s_act} will be smaller than $1/t_s$.

Fig. 19 shows the control structure of ACM-based On time control method.

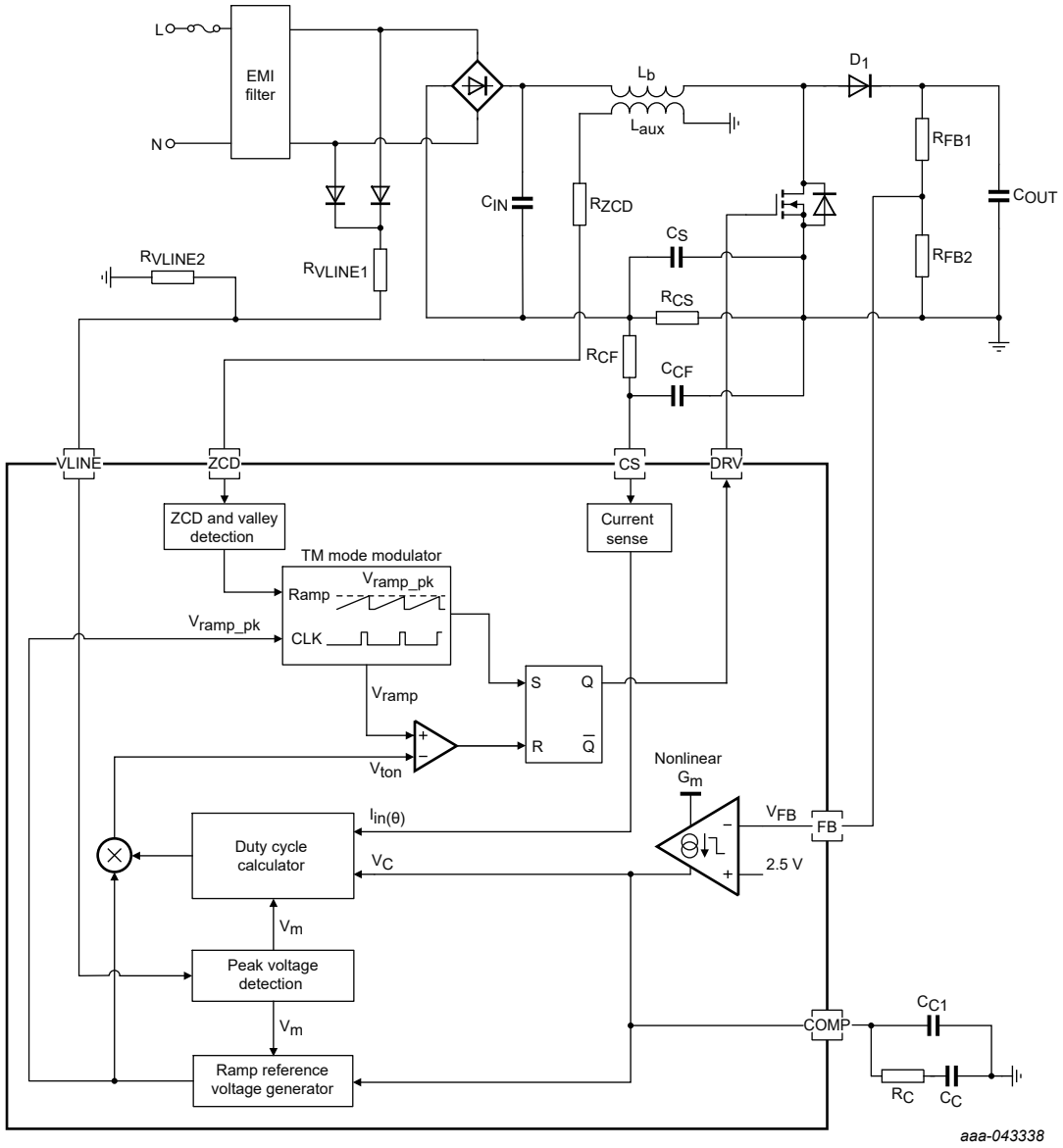


Fig. 19. ACM-based On time control structure

According to equation (3) and Fig. 19, based on the ACM control, the On time is given by

$$V_{t_{on}}(\theta) = \left[1 - \frac{k_r^2 V_m^2 k V_{L\_av}(\theta)}{V_C}\right] V_{ramp\_pk} \quad (4)$$

Where k is the gain of the analog multiplier, k_r is the division resistor ratio for line voltage peak value detection, V_m is the line voltage peak value. The control loop generates V_c, which can be seen as $\frac{kv_o k_r^2 V_m^2 R_{cs}}{R_{in\_eq}}$, the On time is calculated by the actual input current which will track the input voltage. For TM mode, the equation of ramp signal peak value is given by

$$V_{ramp\_pk} = V_{ramp\_pk\_ref} + k_{f\_TM} V_c - k_{l\_TM} k_r V_m \quad (5)$$

Where $V_{ramp\_pk\_ref}$ is 1, k_{f_TM} is 0.75, and k_{l_TM} is 1. Substitute equation (5) into (4), and the On time is given by

$$V_{t_{on}}(\theta) = \left[1 - \frac{k_r^2 V_m^2 k V_{L\_av}(\theta)}{V_c}\right] \left(V_{ramp\_pk\_ref} + k_{f\_TM} V_c - k_{l\_TM} k_r V_m\right) \quad (6)$$

According to equation (6), the peak current is given by

$$i_{pk}(\theta) = \frac{V_{in}(\theta)C_{ch}}{I_{ch}L_b}\left[1 - \frac{k_r^2 V_m^2 k V_{L\_av}(\theta)}{V_c}\right]\left(V_{ramp\_pk\_ref} + k_{f\_TM}V_c - k_{l\_TM}k_r V_m\right) \quad (7)$$

Where C_{ch} is the internal capacitor, I_{ch} is the internal charge current, L_b is the boost inductor. When the PFC controller is operating in CrM, the input current in half line cycle ([0, π]) is given by

$$i_{in}(\theta) = \frac{V_{in}(\theta)C_{ch}}{2I_{ch}L_b}\left[1 - \frac{k_r^2 V_m^2 k V_{cs}(\theta)}{V_c}\right]\left(V_{ramp\_pk\_ref} + k_{f\_TM}V_c - k_{l\_TM}k_r V_m\right) \quad (8)$$

Fig. 20 (a) shows the ideal waveforms under COT control. However, with consideration of the valley switching, the actual waveforms under COT control are shown in Fig. 20 (b).

The inductor current has negative resonant stage which reduces the input current average value and causes severe current distortion. Equation (8) is an ideal theoretical formula without considering the negative resonant. Based on equation (7), the inductor current peak value is not sinusoidal as shown in Fig. 20 (c).

In addition, the input current is approximately regulated to be sinusoidal with consideration of the negative resonant.

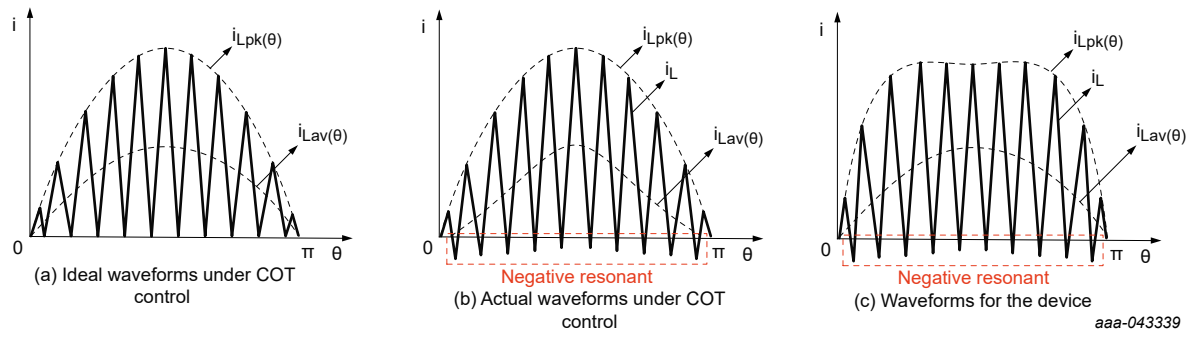


Fig. 20. ACM-based on time control structure

The recommended inductor value and current sense resistor for NEX83288 under different load conditions are shown in Table 10.

Table 10. Recommended inductor value and current sense resistor

Maximum output power (W)	Inductor value (μH)	Current sense resistor (mΩ)
160	200	75
200	170	50
240	130	50
300	110	30

13.3.2. Loop compensation

Fig. 21 shows the small signal equivalent circuit of PFC converter, C is the output capacitor, R_{esr} is the series parasitic resistor, R is the load resistor.

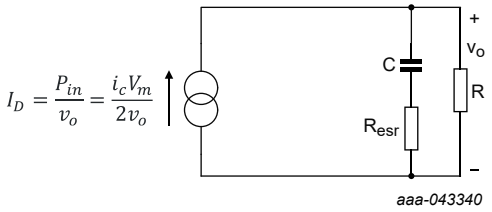


Fig. 21. Small signal equivalent circuit for PFC converter

Based on Fig. 21, the transfer function from V_c to v_o is given by

$$G_{iv}(s) = \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{R}{2kk_r{}^2v_o{}^2R_{cs}} \frac{sR_{esr}C + 1}{s(3R_{esr} + R)C + 3} \approx \frac{R}{6kk_r{}^2v_o{}^2R_{cs}} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \quad (9)$$

There are 1 pole $\omega_z = \frac{1}{R_{esr}C}$ and 1 zero $\omega_p = \frac{3}{RC}$ for PFC converter. Fig. 22 shows the compensation network for NEX83288.The loop control of NEX83288 is based on nonlinear transconductance error amplifier described in Section 13.3.5. Based on the compensation network, the control loop transfer function is given by

$$G_{vv}(s) = \frac{\hat{v}_c(s)}{\hat{v}_o(s)} = \frac{R_{FB2}G_m}{R_{FB1} + R_{FB2}} \frac{sR_CC_C + 1}{sC_C(sR_CC_{C1} + 1)} \quad (C_C >> C_{C1}) \quad (10)$$

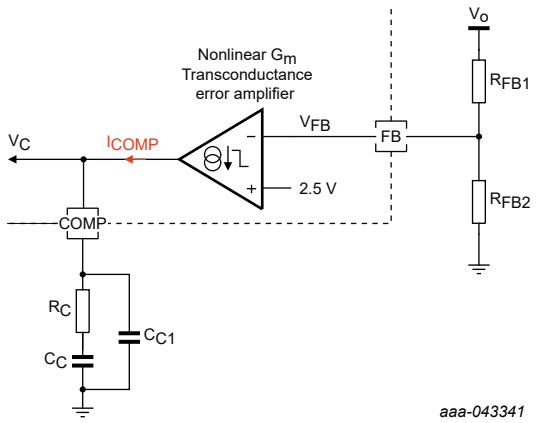


Fig. 22. Loop compensation network

According to the above analysis, we can design the compensation parameters using k-factor method. The recommended compensation parameters under different load conditions are shown in Table 11.

Table 11. Recommended compensation parameters

Maximum output power (W)	R_C (kΩ)	C_C (nF)	C_{C1} (nF)
160	51	680	100
200	68	1000	220
240	33	1000	220
300	22	2200	220

13.3.3. Startup during normal operations

Fig. 23 shows the startup timing of NEX83288. The device is enabled when VCC is higher than the power on threshold V_{VCC_ON} and disabled when VCC drops below the power-off (UVLO) threshold V_{VCC_UVLO}.

Before VCC rises to V_{VCC_ON}, the device is in a UVP or OLP state. After the device is powered on, it will check all the FAULT signals, including brown-in/brown-out and OLP protections. When V_{FB} is higher than the OLP threshold, the device will start a 5 ms delay and then enter the soft start state. During the soft start, the reference voltage rises from the current V_{FB} to 2.5 V and the output voltage slowly rises to the target voltage.

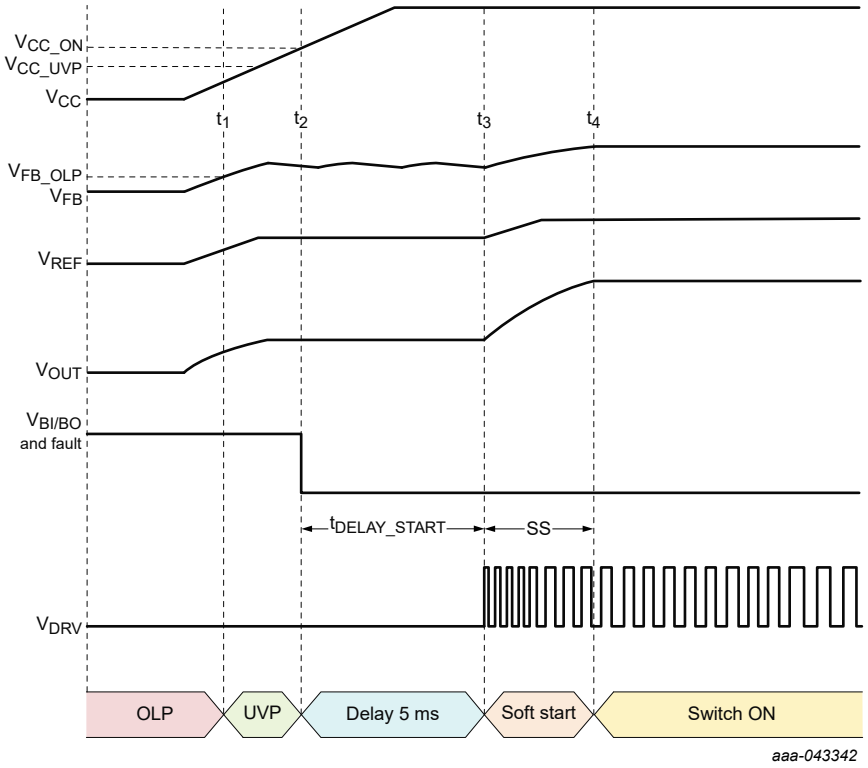


Fig. 23. Startup timing diagram

13.3.4. Brown-in and brown-out

The VLINE pin of NEX83288 supports brown-in and brown-out detection. When the line voltage is continuously higher than the brown-in threshold V_{VLINE_BI} for a debounce time, it is considered that the line voltage is normally connected.

When the line voltage drops continuously below the brown-out threshold V_{VLINE_BO} for 50 ms, it is considered that the line voltage is abnormally connected. Fig. 24 and Fig. 25 show the brown-in/out detection diagram and method respectively.

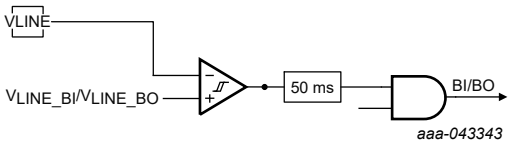


Fig. 24. Brown-in and brown-out detection diagram

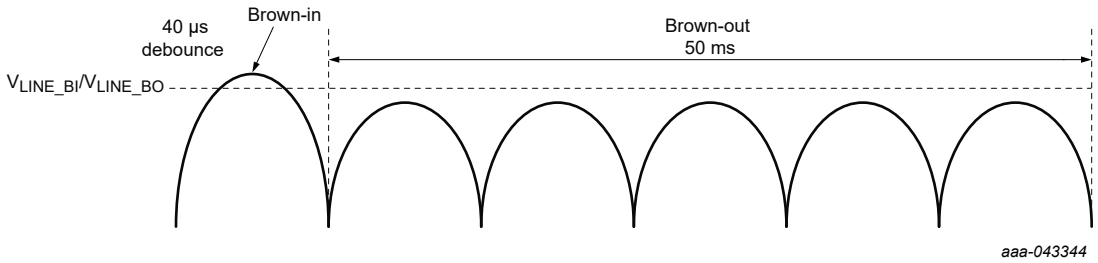


Fig. 25. Brown-in and brown-out detection method

13.3.5. Nonlinear transconductance error amplifier

To improve the dynamic of PFC converter, the device integrates a nonlinear transconductance error amplifier. Fig. 26 shows the nonlinear transconductance error amplifier output current varies with the feedback voltage. When the feedback voltage is lower than 2.1 V, the output current of error amplifier is clamped at 70 µA.

- When the feedback voltage is between 2.1 V and 2.4 V, the equivalent transconduction is 300 µA/V.
- When the feedback voltage is between 2.4 V and 2.6 V, the equivalent transconduction is 100 µA/V.
- The equivalent transconduction will increase to 800 µA/V while the feedback voltage is higher than 2.6 V.

The output current of error amplifier changes according to the feedback voltage, which will charge and discharge the compensation network quickly. This ensures that COMP voltage is quickly pulled down to prevent over-voltage protection (OVP) from being triggered.

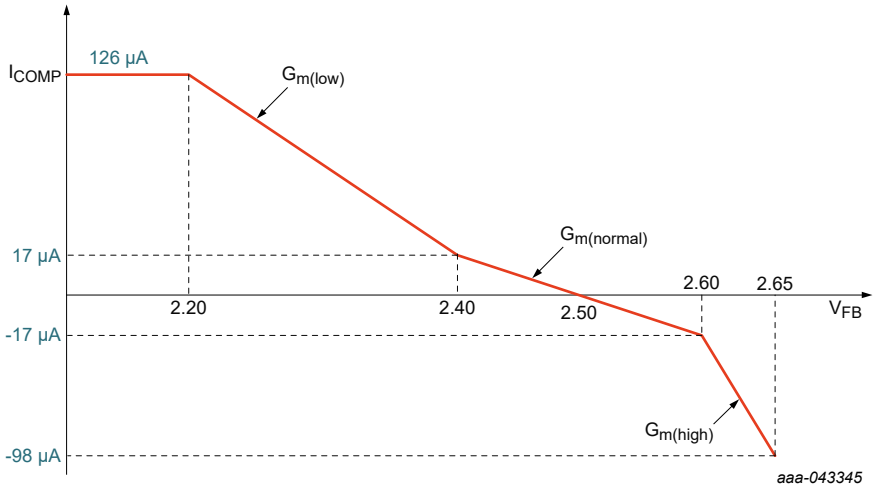


Fig. 26. Nonlinear G_m

13.3.6. Burst mode with soft on or off

Fig. 27 shows the burst mode control diagram.

- When the output voltage is higher than the OVP threshold, the device will shut down the PWM signal until the OVP signal is released. The burst mode is implemented based on the control voltage V_{COMP}.
- When the control voltage V_{COMP} is lower than the burst mode threshold, the device will shut down the PWM signal with five soft-OFF pulses.
- When the control voltage V_{COMP} is higher than the burst mode threshold, the device will release the PWM signal with five soft-ON pulses.

This soft-ON/OFF control avoids abrupt inductor current changes and attenuates the acoustic noise accordingly. During the burst-off period, the device shuts down most of the internal block and ensures that the supply current is below I_Q (typically 460 µA).

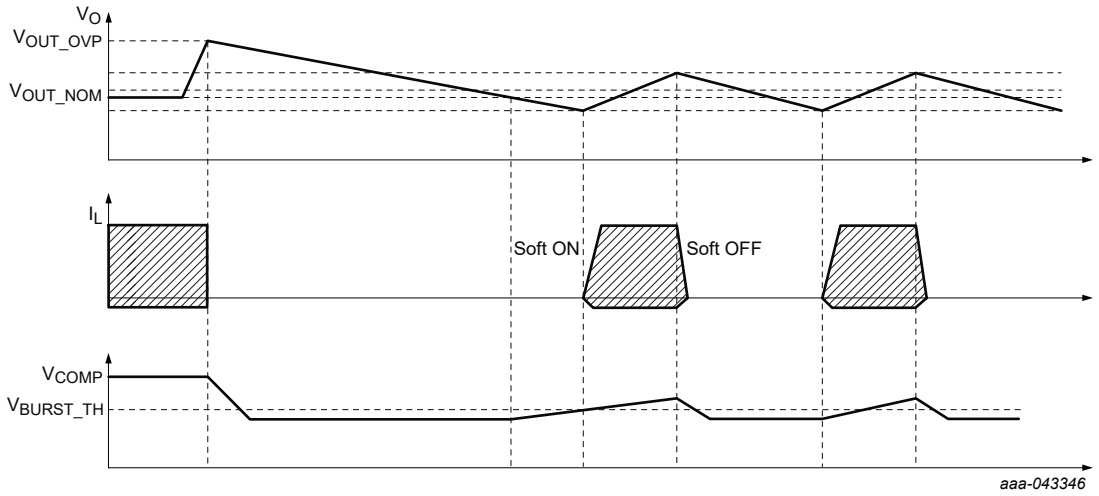


Fig. 27. Burst mode with soft on or off

13.3.7. Zero current detection and valley switching

The zero current detection and valley switching is detected by the auxiliary winding and is implemented by ZCD pin. Fig. 28 shows the structure of zero current detection and valley switching.

The voltage of ZCD pin is upper and lower clamped at 5.7 V and 0.5 V respectively. There are two steps of threshold voltage for ZCD detection, one is for detecting the demagnetization point and the other is for detecting the valley point.

- When the ZCD voltage is lower than the demagnetization threshold voltage V_{ZCD_DETA}, it indicates the inductor current drops to zero.
- When the ZCD voltage is lower than the V_{ZCD_DETT}, it means that the MOSFET drain voltage drops to the valley region.

After a delay time t_{ZCD_DELAY}, the ZCD signal is generated and the MOSFET is turned on at the valley point. Fig. 29 shows the timing diagram of zero current detection and valley switching. The external ZCD resistor is given by

$$R_{ZCD} \geq \frac{V_{L\_aux\_max} - V_{ZCD\_clamp}}{I_{ZCD\_DET}} \quad (11)$$

Where $V_{L\_aux\_max}$ is the maximum voltage on the auxiliary winding, V_{ZCD_clamp} is the upper clamp voltage on ZCD pin, I_{ZCD_DET} is the maximum current on ZCD pin.

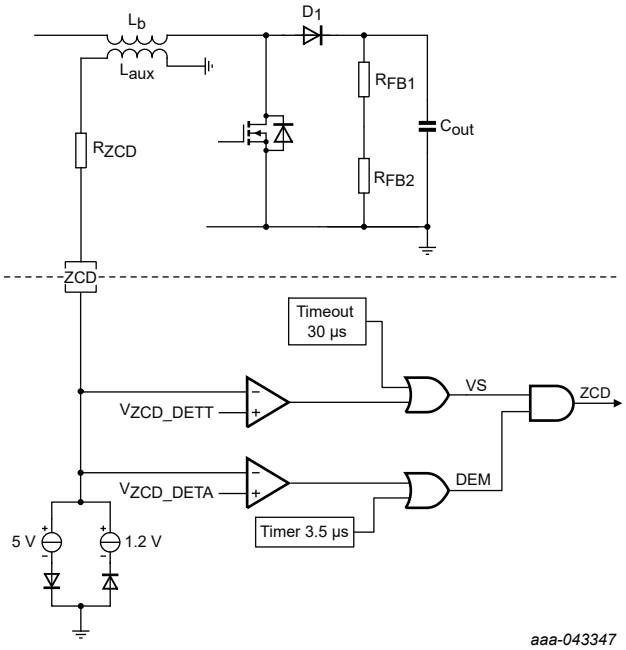


Fig. 28. Structure of zero current detection and valley switching

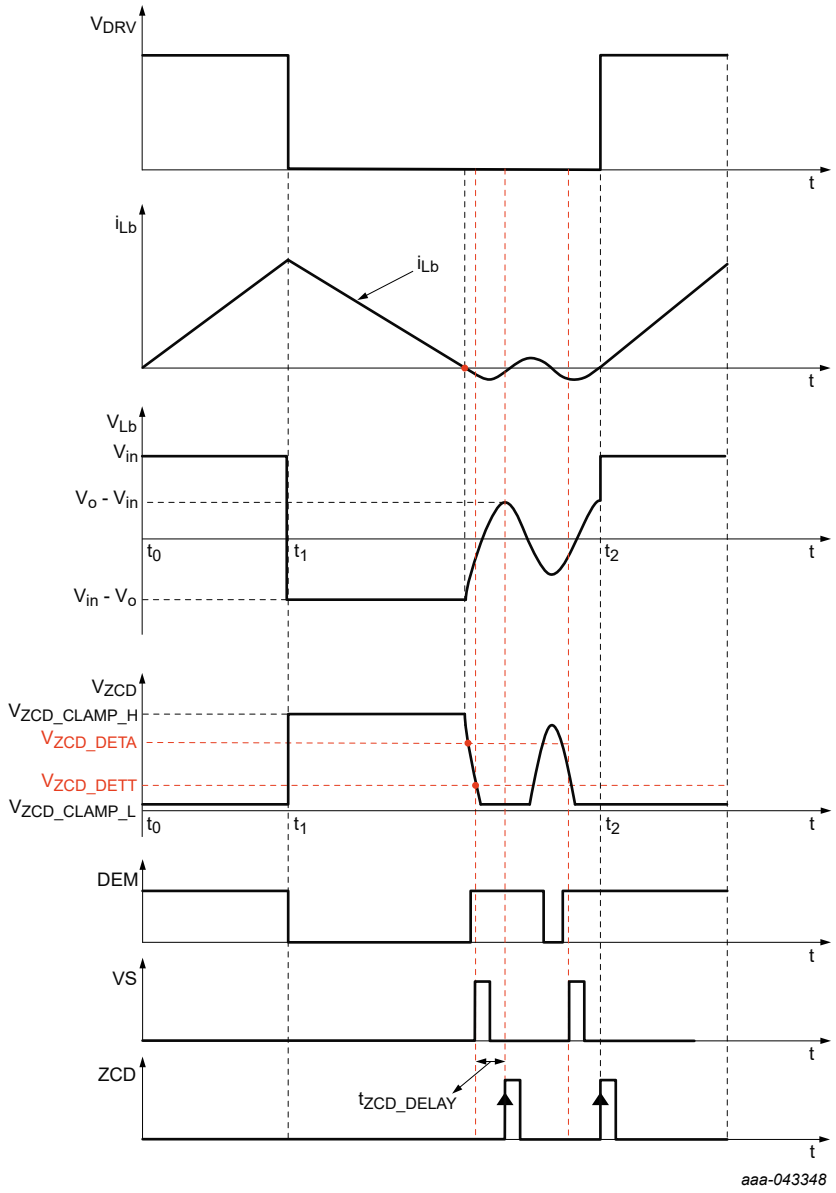


Fig. 29. Timing diagram of zero current detection and valley switching

13.3.8. AC-line drop detection

There is often the case that the AC-line voltage momentarily drops to zero or nearly zero, due to abnormal connection or transient abnormal events affecting the local AC-power distribution network.

During an AC-line dropout, the down-stream power stages depend on sufficient energy storage in the PFC output capacitance, which is sized to provide the ride-through energy for a specified hold-up time. Typically, while the PFC output voltage is falling, the voltage-loop error amplifier output will rise to maintain regulation.

Therefore, the excessive duty cycle is commanded when the AC-line voltage returns, and high peak current surges may saturate the boost inductor with possible overstress and audible noises.

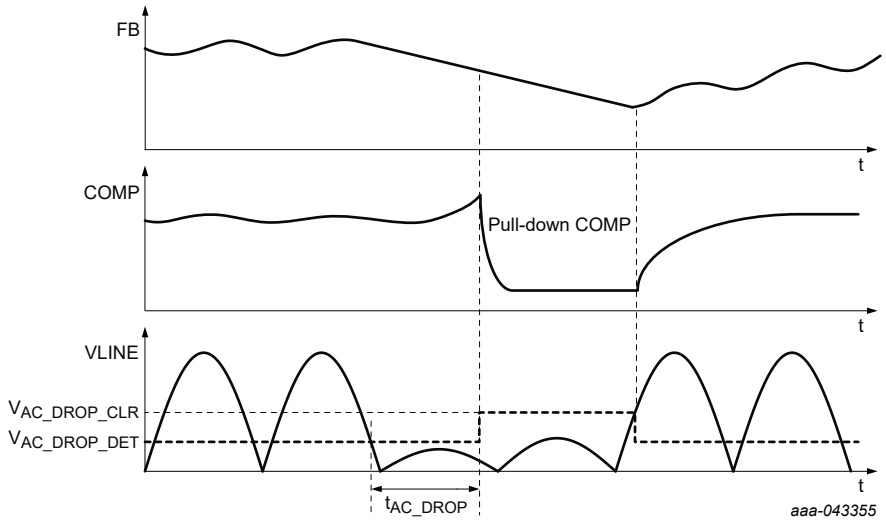


Fig. 30. AC-line dropout timing diagram

NEX83288 supports an AC-line dropout detection function. When detecting the AC-line dropout event, the device will pull down the COMP voltage during the dropout and release the COMP voltage while the AC-line is resumed. If the VLINE voltage falls below $V_{AC\_DROP\_DET}$ for longer than t_{AC_DROP}, a dropout condition is detected, and the error amplifier output is turned off.

Besides, a pull-down current is applied to COMP to gently discharge the compensation network capacitors. In this way, when the AC-line voltage returns, the COMP voltage (and corresponding duty-cycle setting) remains very near to or even slightly below the level that it was before the dropout occurs. Current surges due to excessive duty-cycle, and their undesired attendant effects, are prevented.

13.3.9. Protections

Fig. 31 shows the protections action flowchart. The device supports brown-in/out, overcurrent protection (OCP), inductor saturation protection (ISP), open-loop protection (OLP), VCC overvoltage protection (VCC OVP) and overtemperature protection (OTP). There are three different actions for different protections:

1. For brown-in/out, OLP, OTP, VCC OVP protections, when the fault signal is triggered, the device will shut down PWM output and then discharge VCC to V_{VCC_OFF} and release. If the fault signal does not release, the PWM remains off state and the VCC will charge and discharge between V_{VCC_ON} and V_{VCC_OFF}. When the fault signal is released, the device will enter soft start after 5 ms.
2. For ISP/OCP, when the fault signal is triggered, the action is the same as 1. The only difference is the delay time from fault signal releases to soft start is increased to 200 ms.
3. For OVP, when the fault signal is triggered, the device will shut down the PWM and wait for the OVP signal to release. If the OVP is released, the PWM will be released.

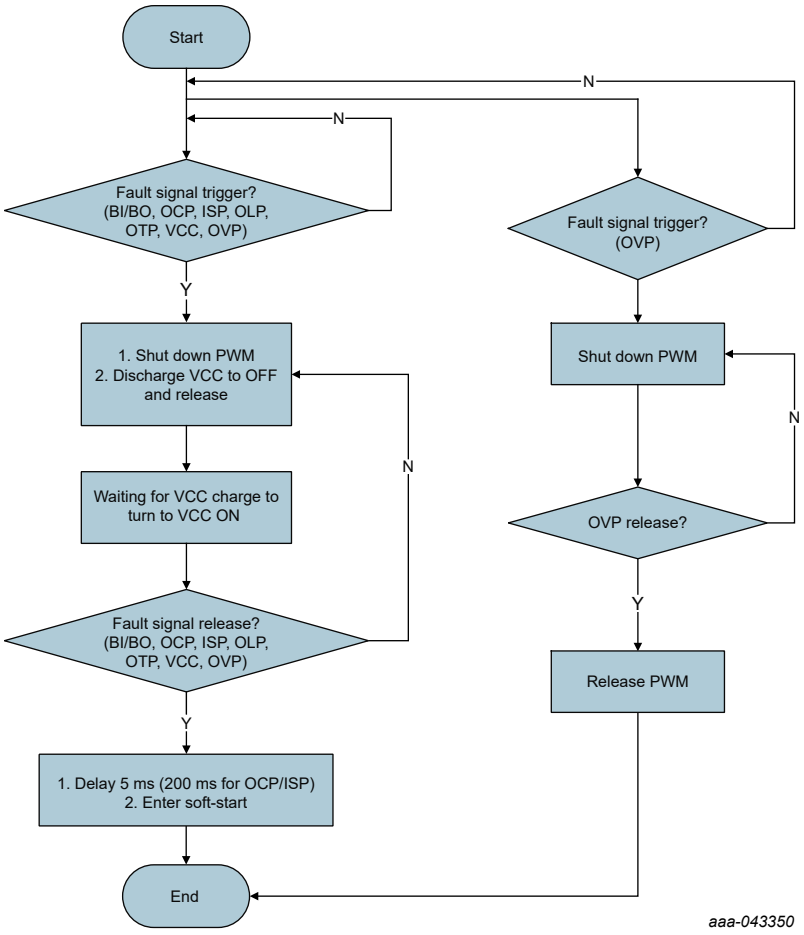
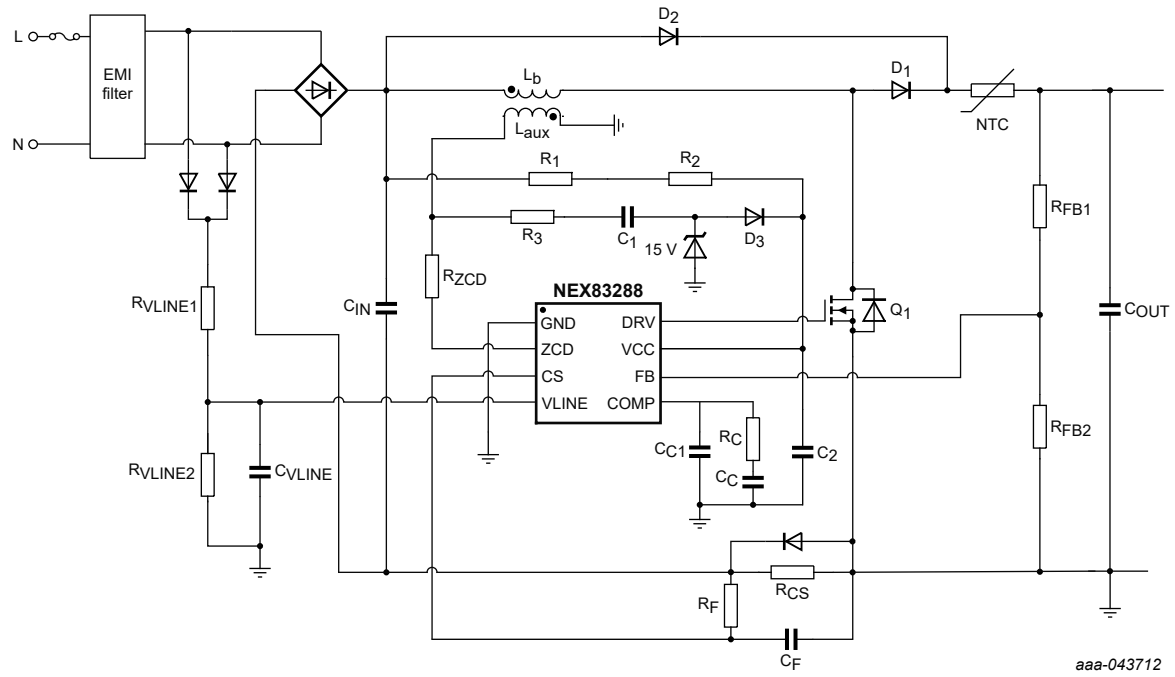


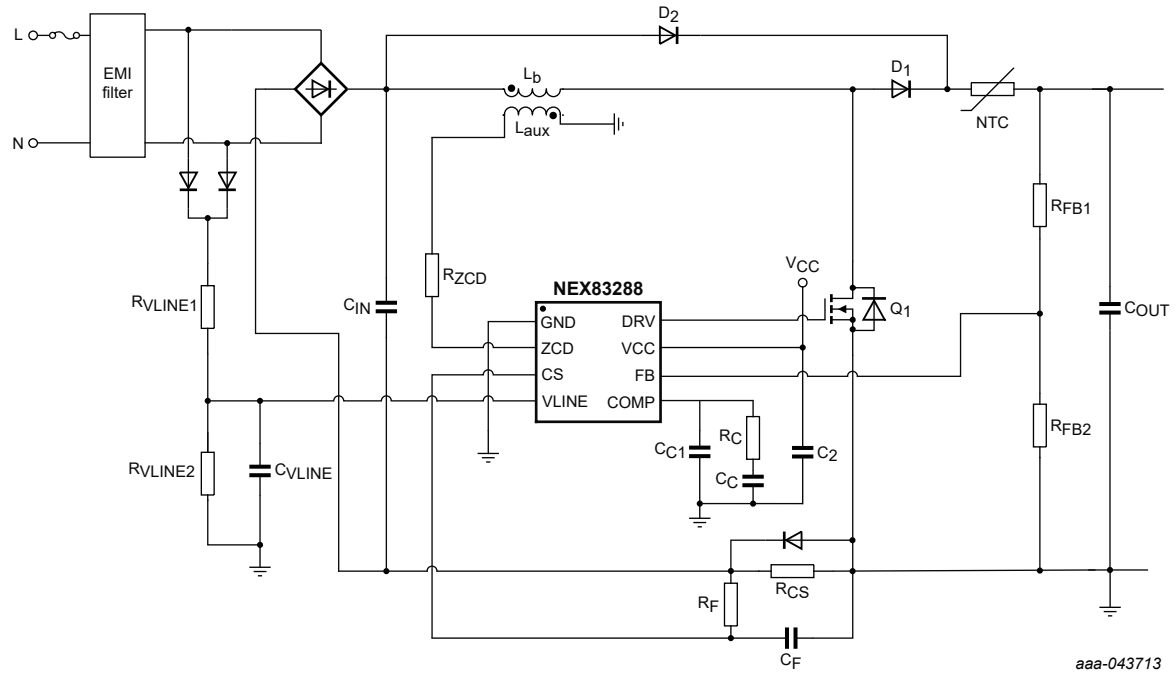
Fig. 31. The work flow of protections

14. Application information

14.1. Typical application



(a) Powered by auxiliary winding



(b) Powered by external VCC

Fig. 32. NEX83288 application circuit

14.2. Design requirements

Table 12 shows the specifications of a 240 W system.

Table 12. System specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
$V_{AC(range)}$	AC voltage range		90	-	264	V
f_{AC}	AC voltage frequency		47	-	63	Hz
V_{VCC_ON}	VCC on		-	12	-	V
V_{VCC_OFF}	VCC off		-	9	-	V
I_{IN}	input current	input = 90 V_{ac}; full load = 240 W	-	2.78	-	A
Output characteristics						
V_{OUT}	output voltage		-	-	400	V
P_L	output power		-	-	240	W
$V_{O(ripple)}$	output ripple		-	12	-	V_{pp}
System characteristics						
η_{peak}	peak efficiency		-	96	-	%

14.3. Power stage design

14.3.1. Rectifier bridge selection

The rectifier bridge is selected considering the maximum instantaneous voltage (the peak value of the line voltage) and the maximum input RMS current can be calculated by equation (12).

$$I_{AC\_MAX} = \frac{P_O}{\eta \times V_{AC\_MIN}} = 278 \quad A \tag{12}$$

The maximum peak input voltage is calculated by

$$V_{in\_max} = \sqrt{2} \times V_{AC\_MAX} = 373 \quad V \tag{13}$$

A standard 600 V/6 A rectifier bridge can be selected to provide enough margins.

14.3.2. Input capacitor selection

The input capacitor behind the rectifier bridge is used to provide a bypass path for the high switching frequency current, and to suppress the ripple on the rectified sinusoidal input voltage.

Generally, 5% to 20% ripple on the input capacitor may be expected. Since the energy stored in the input capacitor is approximately equal to the energy transferred to the load in each switching cycle, equation (14) can be obtained:

$$\frac{1}{2}C_{in}\left(V_{AC\_MIN} + \frac{1}{2}rV_{AC\_MIN}\right)^2 - \frac{1}{2}C_{in}\left(V_{AC\_MIN} - \frac{1}{2}rV_{AC\_MIN}\right)^2 = \frac{P_O}{2\pi f_s} \tag{14}$$

where r is the ripple coefficient. Based on equation (14), the input capacitor can be calculated with equation (15):

$$C_{in} = \frac{P_O}{2\pi f_s \times r \times V_{AC\_MIN}^2} = \frac{I_{AC\_MAX}}{2\pi f_s \times r \times V_{AC\_MIN}} \tag{15}$$

Select a capacitor with good high-frequency performance, such as a film capacitor. Assume that the ripple coefficient is 0.1, the input capacitor can be calculated with equation (16):

$$C_{in} = \frac{I_{AC\_MAX}}{2\pi f_s \times r \times V_{AC\_MIN}} = 0.49 \quad \mu F \tag{16}$$

Two 0.33 µF film capacitors with a 450 V voltage rating are recommended as the input capacitors because they provide high-frequency energy during the switching cycle.

14.3.3. Boost inductor design

The boost inductor value is required to ensure that the maximum load can be delivered from the minimum input voltage, which can be calculated with equation (17):

$$L_{b\_max} \approx \frac{\eta \times V_{AC\_MIN}^2 \times 3.56}{2P_o} \times \frac{2 \times (1.5 + 0.75V_c - k_r V_m)}{\pi} \tag{17}$$

The unit of equation (17) is µH. Assume that V_{COMP} is 3.2 V at full load, the inductor value is

$$L_{b\_max} \approx \frac{\eta \times V_{AC\_MIN}^2 \times 3.56}{2P_o} \times \frac{2 \times (1.5 + 0.75V_c - k_r V_m)}{\pi} = 111.41 \quad \mu H \tag{18}$$

The inductor value can be set as 110 µH.

14.3.4. MOSFET selection

The current rating of MOSFET is determined by the maximum RMS value of the current following through the MOSFET. To calculate the RMS current of MOSFET in each half line cycle, we need to calculate the RMS current of MOSFET in each switching cycle first.

For TM mode, the RMS current of MOSFET in each switching cycle can be estimated with

$$I_{QRMS\_TM}(\theta) = \frac{i_{Lpk}(\theta)}{\sqrt{3}}\sqrt{\frac{T_{on}}{T_s}} = \frac{i_{Lpk}(\theta)}{\sqrt{3}}\sqrt{1 - \frac{v_{in}(\theta)}{v_{out}}} \tag{19}$$

Based on equation (19), the RMS value of MOSFET in each half line cycle can be calculated with

$$I_{QRMS\_TM} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{i_{Lpk}(\theta)}{\sqrt{3}}\sqrt{1 - \frac{v_{in}(\theta)}{v_{out}}}\right]^2 d\theta} = 2\sqrt{2}\, i_{in\_rms}\sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\frac{\sin(\theta)^2}{3} - \frac{\sqrt{2}\, v_{in\_rms}\sin(\theta)^3}{3v_{out}}\right)d\theta} \tag{20}$$

Simplify the formula to obtain equation (21)

$$I_{QRMS\_TM} = 2\sqrt{2}\, i_{in\_rms}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}\, v_{in\_rms}}{9\pi v_{out}}} \tag{21}$$

The RMS current of MOSFET is

$$I_{QRMS\_TM} = 2\sqrt{2} \times I_{AC\_MAX}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times V_{AC\_MIN}}{9\pi \times v_{out}}} = 2.74 \quad A \tag{22}$$

Additionally, the MOSFET pulsed-drain current should exceed the peak inductor current, calculated with equation (23):

$$I_{Q\_Pulse} > 2\sqrt{2}\, I_{AC\_MAX} = 7.86 \quad A \tag{23}$$

14.3.5. Boost diode selection

For TM mode, the average current of diode is equal to the output current. The RMS current of the diode is calculated with equation (24):

$$I_{DRMS\_TM} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{i_{Lpk}(\theta)}{\sqrt{3}}\sqrt{\frac{v_{in}(\theta)}{v_{out}}}\right]^2 d\theta} = 2\sqrt{2}\, i_{in\_rms}\sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{\sqrt{2}\, v_{in\_rms}\sin(\theta)^3}{3v_{out}}d\theta} \quad (24)$$

Simplify the formula to obtain equation (25):

$$I_{DRMS\_TM} = 2\sqrt{2}\, i_{in\_rms}\sqrt{\frac{4\sqrt{2}\, v_{in\_rms}}{9\pi v_{out}}} = 1.67 \quad A \quad (25)$$

The boost diode must have average and RMS current ratings that exceed I_{DAVG} and I_{DRMS}, respectively.

14.3.6. Output capacitor selection

When selecting the output capacitor, we need to consider the following conditions: the output voltage ripple (V_{O_PP}), ripple current rating, and hold-up time. The output ripple is a function of the effective series resistance (ESR) of the output capacitor, the output voltage, and the line frequency (f_L). Based on the energy balance, the energy on the output capacitor is given by

$$P_C(t) = v_{out} i_c(t) = P_{in}(t) - P_o = 2I_{in\_rms}V_{in\_rms}[\sin(\omega_L t)]^2 - P_o = 2P_o[\sin(\omega_L t)]^2 - P_o \quad (26)$$

Based on equation (26), the current following to the output capacitor is calculated by

$$i_c(t) = 2I_o[\sin(\omega_L t)]^2 - I_o = -I_o\cos(2\omega_L t) \quad (27)$$

Considering the ESR of output capacitor, the output ripple is calculated by

$$V_{o\_pp} = 2 \times \frac{P_o}{v_{out}} \times \sqrt{R_{esr}{}^2 + \frac{1}{(2 \times 2\pi f_L \times C_o)^2}} \quad (28)$$

In this case, the calculated ripple with the selected capacitor should be below 3% of the output voltage, and the ESR of the output capacitor is assumed to be 1 Ω. C_O can be calculated by

$$C_o \geq \frac{1}{2 \times 2\pi f_L \sqrt{\left(\frac{3\% \times v_{out}{}^2}{2 \times P_o}\right)^2 - R_{esr}{}^2}} = 160 \quad \mu F \quad (29)$$

In this example design, an aluminum electrolytic capacitor with specification of 180 µF/450 V is recommended.

For TM mode, the maximum RMS ripple current flowing in the output capacitor can be estimated with equation (30).

$$I_{o\_ripple\_max} = \sqrt{I_{DRMS\_TM}{}^2 - \left(\frac{P_o}{v_{out}}\right)^2} = 1.56 \quad A \quad (30)$$

This current flowing into the output capacitor is made up of a double line frequency ripple component (2 x f_L) and a switching frequency component (f_{sw}), calculated with equation (31) and equation (32), respectively.

$$I_{o\_ripple\_100Hz} = \frac{P_o}{\sqrt{2}\, v_{out}} = 0.424 \quad A \quad (31)$$

$$I_{o\_ripple\_fsw} = \sqrt{I_{o\_ripple\_max}{}^2 - I_{o\_ripple\_100Hz}{}^2} = 1.501 \quad A \quad (32)$$

The capacitor should be chosen so that the hold-up time satisfies the relationship calculated with equation (33):

$$C_o = \frac{2 \times P_o \times t_{hold}}{\eta \times (v_{out}{}^2 - v_{out\_hold}{}^2)} \quad (33)$$

Where V_{OUT} is the minimum output voltage under normal operating conditions, and v_{OUT_hold} is the required minimum operating output voltage to supply the second stage DC-DC converter when the line voltage is shut down.

14.4. Control circuit design

14.4.1. FB section

The internal reference voltage V_{REF} is 2.5 V (typical), based on the internal reference voltage, the resistor division ratio is calculated with

$$\frac{R_{FBDWN}}{R_{FBUP} + R_{FBDWN}} \times v_{out} = V_{REF} \quad (34)$$

Since the division resistor will affect the standby power, the selection of resistance value needs to consider standby power consumption. It is recommended that the upper resistor is set as 6.6 mΩ. Based on equation (34), the lower resistor can be calculated with

$$R_{FBDWN} = \frac{V_{REF}}{v_{out} - V_{REF}} \times R_{FBUP} \quad (35)$$

14.4.2. VLINE section

Considering the brown-in and brown-out threshold, the resistors on VLINE pin can be calculated with equation (36).

$$\frac{R_{LDWN}}{R_{LUP} + R_{LDWN}} \times V_{in\_pk} = V_{BRI} \quad (36)$$

Since the division resistors also affect the standby power, the selection of resistance value needs to consider standby power consumption. It is recommended that the upper resistor is set as 6.6 mΩ. Based on equation (37), the lower resistor can be calculated with

$$R_{LDWN} = \frac{V_{BRI}}{V_{in\_pk} - V_{BRI}} \times R_{LUP} \quad (37)$$

14.4.3. ZCD section

The external ZCD resistor is given by

$$R_{ZCD} \geq \frac{V_{L\_aux\_max} - V_{ZCD\_clamp}}{I_{ZCD\_DET}} \quad (38)$$

Where $V_{L\_aux\_max}$ is the maximum voltage on the auxiliary winding, V_{ZCD_clamp} is the upper clamp voltage on ZCD pin, I_{ZCD_DET} is the maximum current on ZCD pin.

14.4.4. CS section

CS is used for CBC and control. The current flowing through the MOSFET should be below the CBC threshold. The CS resistor value can be estimated with equation (39):

$$R_{CS} \leq \frac{V_{CBC}}{2\sqrt{2} \times I_{AC\_MAX}} \quad (39)$$

In this case, the calculated CS resistor is 63.6 mΩ, the resistor can be selected as 50 mΩ. To suppress the spike and improve the control reliability, a low pass filter (220 Ω + 220 pF) is recommended to be added on CS.

14.4.5. COMP section

The compensation parameters can be calculated by the k-factor method. The k-factor method design steps are as follows:

1. For maximum phase Boost at the gain cross-over frequency, compensator design proceeds by placing the pole and zero an equal distance above and below the gain cross-over frequency (f_c) on the bode plot. That is

$$\begin{cases} f_{z1} = \frac{f_c}{k} \\ f_{p1} = f_c \times k \end{cases} \tag{40}$$

2. The system phase at the gain cross-over frequency is given by

$$\emptyset_{PS} = arctan\left(\frac{f_c}{f_z}\right) - arctan\left(\frac{f_c}{f_p}\right) \tag{41}$$

Based on equation (40) and (41), the open loop transfer function is

$$G_{iv}(s)G_{vv}(s) = \frac{R}{6kk_r{}^2v_o{}^2R_{cs}} \frac{R_{FB2}G_m}{R_{FB1}+R_{FB2}} \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \frac{1+\frac{s}{\omega_{z1}}}{sC_C\left(1+\frac{s}{\omega_{p1}}\right)} \tag{42}$$

Where $\omega_{z1} = 2\pi f_{z1} = \frac{1}{R_C C_C}$ and $\omega_{p1} = 2\pi f_{p1} = \frac{1}{R_C C_{C1}}$.
The compensator expected phase boost of the compensator is given by

$$\emptyset_{boost} = \emptyset_{PM} - \emptyset_{PS} - \frac{\pi}{2} = arctan\left(\frac{f_c}{f_{z1}}\right) - arctan\left(\frac{f_c}{f_{p1}}\right) = arctan(k) - arctan\left(\frac{1}{k}\right) \tag{43}$$

Furthermore, since $arctan(k) + arctan\left(\frac{1}{k}\right) = \frac{\pi}{2}$, k can be derived from equation (44)

$$k = \tan\left(\frac{\emptyset_{PM} - \emptyset_{PS}}{2}\right) \tag{44}$$

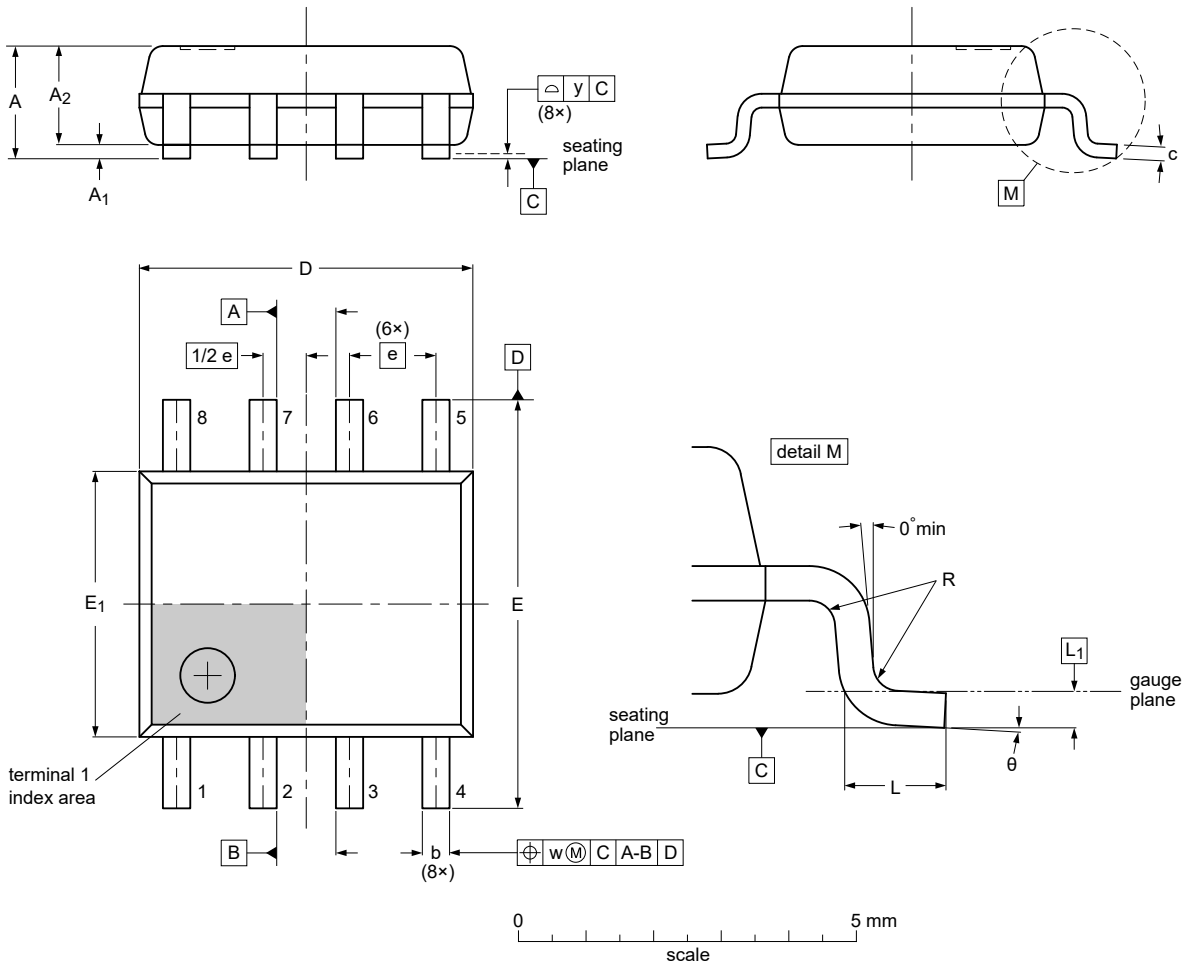
3. R_C, C_C and C_{C1} are calculated by the system gain at cross over frequency:

$$\begin{cases} C_C = \frac{R}{6kk_r{}^2v_o{}^2R_{cs}} \frac{R_{FB2}G_m}{R_{FB1}+R_{FB2}} \frac{k}{2\pi f_c} \sqrt{\frac{1+\left(\frac{f_c}{f_z}\right)^2}{1+\left(\frac{f_c}{f_p}\right)^2}} \\ R_C = \frac{k}{2\pi f_c C_C} \\ C_{C1} = \frac{1}{2\pi k f_c R_C} \end{cases} \tag{45}$$

Select the appropriate gain cross-over frequency f_c (< 20 Hz) and phase margin ϕ_{PM} (≥ 65 °C), the compensator parameters can be calculated by equation (45). In this case, the recommended compensation parameters are C_C = 1 µF, R_C = 33 kΩ, C_{C1} = 220 nF.

15. Package outline

Plastic, small outline package; 8 leads; 1.27mm pitch; 4.9 mm x 3.9 mm x 1.75mm body **SOT96-2**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	L	L_1	R	w	y	θ
mm	max	1.75	0.25	1.55	0.51	0.25	5.10	6.20	4.00	1.27 BSC	1.27	0.25 BSC	0.15 REF	0.25	0.10	8°
	nom															
	min	1.45	0.10	1.35	0.33	0.17	4.70	5.80	3.80		0.40					0°

Note
1. Dimension D does not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burr shall not exceed 0.15 mm per end. Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

sot96-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT96-2						25-03-12

Fig. 33. Package outline SOT96-2 (SO8)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
AC	Alternating Current
ACM	Average Current Mode
ANSI	American National Standards Institute
BI	Brown-in
BO	Brown-out
CCM	Continuous Conduction Mode
CDM	Charged Device Model
CrM	Critical Conduction Mode
COT	Constant On Time
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
GaN	Gallium Nitride
HBM	Human Body Model
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
ISP	Inductor Saturation Protection
JEDEC	Joint Electron Device Engineering Council
LCD	Liquid Crystal Display
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCP	OverCurrent Protection
OLP	Open Loop Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PFC	Power Factor Correction
PWM	Pulse-Width Modulation
THD	Total Harmonic Distortion
TM	Transition Mode
UVLO	Under-Voltage LockOut
UVP	UnderVoltage Protection
VOT	Variable On Time

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX83288 v. 1.1	20250916	Product data sheet	-	NEX83288 v. 1
Modifications:	• Fig. 18: Functional block diagram updated. • Table 12: The symbol of peak efficiency updated. • Fig. 33: Package outline drawing updated.			
NEX83288 v. 1	20250821	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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